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# VLSI Fuzzy Cells

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## 1. Abstract

This work presents excellent basic cells for the construction of logic Trapezoidal Membership Functions (TMF). The proposed cell is composed of the following: current subtract circuit, multiplier/divider and the S-Z shapes circuit. All the circuits presented in this paper use CMOS 0.18 m technology and work in current-mode. The efficient performance achieved in this work is demonstrated, first, by the individual simulation of the new cells and, second, by the implementation of a decision making system that uses the Mamdani inference method and the new TMF cells as the knowledge base. It is important to mention that maximum and minimum circuits were used for the implementation of the Mamdani inference method. The key objective of this work is to demonstrate that the improved cells presented are suitable for the implementation of a decision making system based on a fuzzy logic inference method.

**Palabras clave:** lógica difusa, funciones de membresía, diseño VLSI, sistemas para toma de decisiones.

## 2. Resumen (Celdas difusas en VLSI)

Este trabajo presenta el desarrollo de celdas básicas para la construcción de funciones de membresía trapesoidales, TMF. Las celdas TMF se encuentran formadas por un circuito de sustracción de corriente, un multiplicador/divisor, y circuitos de forma S-Z. Todos los circuitos presentados en este artículo usan tecnología CMOS de 0.18 µm y trabajan en modo de corriente. El eficiente funcionamiento de las celdas presentadas en este trabajo se demuestra, primero, por medio del funcionamiento independiente de cada una de las celdas nuevas y, segundo, por medio de la realización de un sistema de toma de decisión que emplea el método de inferencia de Mandani junto con las nuevas celdas como base de conocimiento. Es importante mencionar que circuitos de máximo y mínimo fueron usados para el desarrollo del método de inferencia de Mamdani. El objetivo principal de este trabajo es demostrar que las celdas mejoradas son susceptibles para la realización de sistemas de toma de decisiones basados en el método de inferencia de la lógica difusa.

**Key words:** logic, membership functions, VLSI design, decision making systems.

## 3. Introduction

Fuzzy logic allows the manipulation of information that handles certain degree of membership in a fuzzy array and permits its representation by means of a characteristic membership function. These functions can be related with others, with the use of linguistic variables, in a fuzzy rule that allows the obtention of a conclusion from vague or uncertain information.

The digital and analog techniques constitute the two existent approaches for the hardware realization of fuzzy systems. The features of these techniques make ones more suitable than the other in specific applications.

Nevertheless, for the realization of an efficient fuzzy system, it is required that both techniques contemplate in its design the available time for the rule processing, the space to be occupied by the system and the power it must consume.

The digital approach has a high degree of programmability, but it requires of an analog-digital and digital-analog converters for the interaction with the physical variables that the system works with, besides this turns the system into an array that occupies a considerably great amount of space.

In the contrary way, the analog arrays count with a higher degree of difficulty to be programmed, but in terms of space occupation they are more effective arrays because of the

reduced number of transistors necessary. Analog systems are preferred for its higher processing velocity and its reduced power consumption. Nevertheless, they present certain disadvantages in comparison with the digital systems, the lack of facility to use CAD (Computer Aided Design) tools for its design, and its mayor sesitivity to noise and distortion.

Digital systems must struggle with a lot of problems to minimimize the calculus time and the area consumption [14]. Therefore, investement has been done in the research of methods that allow the solution of these problems, without the necessity of the development of dedicated hardware that needs to be adapted for a spedific problem [13]. This diminishes the functionality of the digital systems and highlights the necessity to develop fuzzy systems that operate in analog form.

In the other hand, analogous systems present topologies that in terms of complexity and space result quite efficient, but with a low programmability [8], [9], [10]. There are works that offer more complex systems, that present a higher programmability degree [3],[11], [12]. Nevertheless, many of these designs must be improved in order for them to work in the most efficient way in terms of fuzzy logic; this is the case specificly speaking of the work presented in [3]. The topology presented by Camacho in his work offers a clear advantage over the other proposed designs, and this is the generation of asymmetric and symmetric membership functions. Because of this reason, the work of Camacho is taken as the basis for the development of a fuzzy system that operates in an efficient form using Camacho´s TMF circuit for the construction of the system´s knowledge base.

In regard to analog fuzzy system design, we considered that for this work the best option was to use circuits that operated in current-mode, since the implementation for the functions of substraction, addition, multiplication, division, minimum and maximum can be done in a simpler way using current mirrors. To this we must add that the current-mode integrated circuits are less sensitive to temperature, they are robust to technology scaling, they are capable to operate with low voltage feeding and they can interact with various sensors [1].

The parameters that can be programmed in a fuzzy integrated circuit include the number of fuzzy arrays that will cover the antecedent rule; the parameters define it´s membership functions, the number of arrays for the consequent rules, and the parameters that highlight the rule base.

The key objective of this work is to take the cells that constitute the units that generate the fuzzy logic membership functions and make the appropiate changes to their structure, so they can operate with the most efficient performance possible in terms of fuzzy logic operation. The improved performance of these cells will be proved via the simulation of a decision making system that uses the Mamdani inference method and the new TMF cells as the knowledge base.

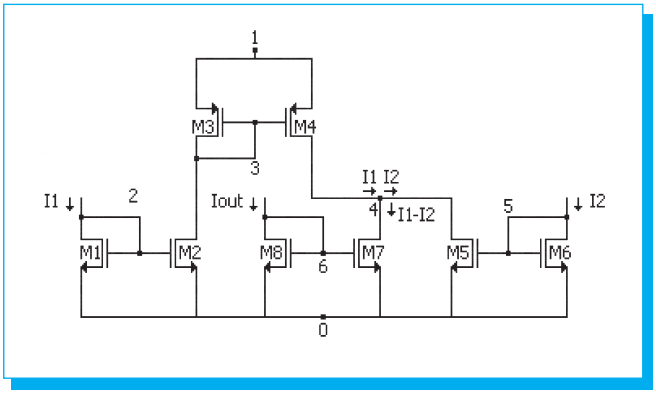


**Fig. 1.** Current subtract circuit.

## 4. Development

### 4.1 Individual Cells

In this section, we will present the different cells needed for the construction of the TMF cell. We will start with the current substractor, then we will pass to the description of the multiplier/divider, and finally we will proceed with the cell that allows us the construction of *S* and *Z* forms.

*A. Current Subtract Circuit*

The current subtract circuit proposed in [3] is the one presented in Fig. 1. This circuit is in charge of the subtraction of current $I_2$ from $I_1$. While $I_1 > I_2$ the circuit's output current is the result of the subtraction and when $I_1 \leq I_2$ the output is equal to zero. Equation (1) represents the transfer function of the current substractor in terms of the dimensions of the transistors it uses.

$$I_{out} = \begin{cases} \dfrac{L_{M7}W_{M8}}{L_{M8}W_{M7}}\left[ -\dfrac{L_{M6}W_{M5}}{L_{M5}W_{M6}} I_2 \right], & I_1 \\ , & I_1 \end{cases} \quad (1)$$

If the geometrical relationships of all the transistors are kept unitary, then (1) reformulated as

$$I_{out} = \begin{cases} I_1 - I_2 \\ 0 \end{cases} \quad (2)$$

**Table 1.** Modified geometrical relationships.

| Transistor | Camacho [3] | Work |
|---|---|---|
| $M_1$ | $10\mu/10\mu$ | $1.8\mu/0.36\mu$ |
| $M_2$ | $10\mu/10\mu$ | $1.8\mu/0.36\mu$ |
| $M_3$ | $10\mu/10\mu$ | $3.6\mu/0.36\mu$ |
| $M_4$ | $10\mu/10\mu$ | $3.6\mu/0.36\mu$ |
| $M_5$ | $10\mu/10\mu$ | $1.8\mu/0.36\mu$ |
| $M_6$ | $10\mu/10\mu$ | $1.8\mu/0.36\mu$ |
| $M_7$ | $10\mu/10\mu$ | $0.36\mu/3.6\mu$ |
| $M_8$ | $10\mu/10\mu$ | $0.36\mu/3.6\mu$ |

The mirrors formed by transistors $M_1$, $M_2$, $M_3$ and $M_4$ are in charge of introducing current $I_1$ into node 4. The transistors $M_5$ and $M_6$ extract current $I_2$ from node 4. The result of the substraction is taken from node 4 by the mirror formed by $M_7$ and $M_8$. This mirror is in charge also of preventing the output current from being negative; this is the reason why the output current is equal to zero when $I_1 \leq I_2$ .

The original substraction circuit presented in [3] had the geometrical relationships for every transistor randomly chosen. This caused a load decompensation between the

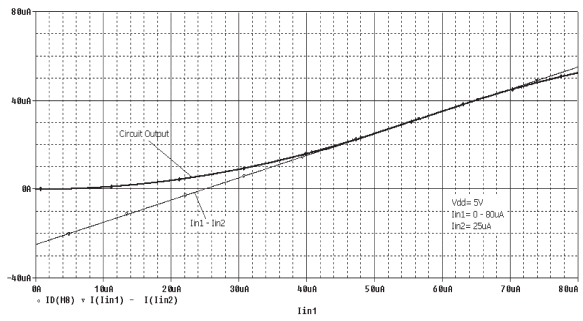


**Fig.2.** Simulation output presented in [3].

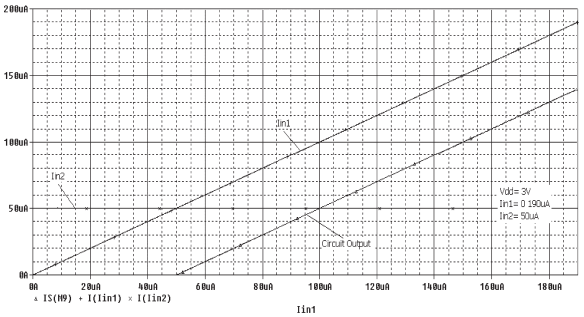


**Fig. 3.** Simulation output presented in this work.

mirror composed by transistors $M_5$ and $M_6$, and the mirror made by $M_7$ and $M_8$. Table 1 shows a comparison between the original dimensions and the geometrical relationships considered in this work for a more efficient performance.

The performance of the substractor circuit described with anteriority was tested using the PSPICE circuit simulator. In this case, Fig. 2 shows the circuit´s simulation output using Chamacho´s transistor model AMS 0.8 µm and the geometrical relationships of Table 1 presented in his work. As it can be seen, there is a significant error in the current subtract circuit's output.

In order to improve the performance of the circuit, we used the proposed geometrical relationships stated in Table 1 and we changed the transistor model to MOSIS 0.18 µm. Fig. 3 depicts the output of the subtraction circuit under the new simulation conditions. After the pertinent modifications we reduced the consumption area, minimized the output error and incremented the dynamic range of the circuit from 0-70 µA ($V_{dd}$ = 5 V) to 0-190 µA ($V_{dd}$ = 3 V).

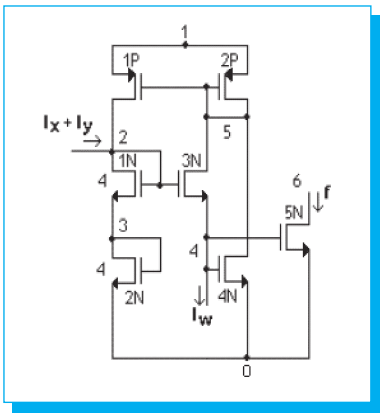


**Fig. 4.** Basic Tranlinear Cell presented in [4].

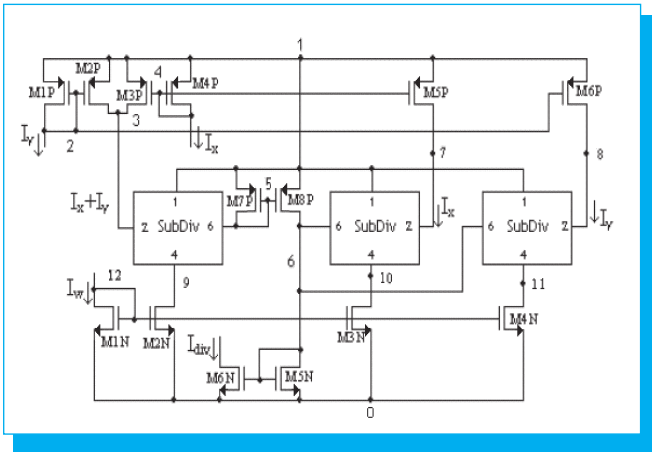


**Fig. 5.** Quadratic-translinear multiplier/divider.

*B. Multiplier/Divider*

The multiplier/divider presented in [3] is based on the *Generalized Translinear Principle* proponed in [4]. With the help of this principle it is possible to perform the next operation:

$$I_{out} = \frac{I_x I_y}{I_w} = \left( \left( I_x + I_y \right)^2 - I_x^{\,2} - I_y^{\,2} \right) \Big/ 2I_w \qquad (3)$$

Equation (3) represents the desired output function for the multiplier/divider. Using the generalized translinear principle we were able to perform the wanted output function using a series of operations described next. We applied this principle for the creation of a basic tranlinear cell used by the multiplier/divider.

The generalized translinear principle is based on Kirchoff´s Voltage Law, which states that the algebraic addition of all the voltages $V_{GS}$ of a loop formed by MOS transistors must be equal to zero, therefore, considering the characteristic quadratic equation of the MOS transistors, we have that [4]

$$\sum_{CW} \sqrt{\frac{I_D}{\frac{W}{L}}} = \sum_{CCW} \sqrt{\frac{I_D}{\frac{W}{L}}} \qquad (4)$$

To analyze the basic translinear cell of Fig. 4 we must depart from the function proposed in equation (5).

$$\sqrt{f} + \sqrt{I_W} = 2\sqrt{\left( f + I_W + I_{in} \right.} \qquad (5)$$

This equation is obtained by applying KVL to the loop formed by transistors $M_{1N}$, $M_{2N}$, $M_{3N}$ and $M_{4N}$ of Fig. 4. It can be appreciated, that it has the form of equation (4). If we raise to the second power both sides of equation (5) and solve for $f$, we reach the function modeled by equation (6).

$$f = \frac{(I_{in})^2}{4I_w} \qquad (6)$$

The circuit of Fig. 4 represents the basic translinear cell. This cell performs the function described by equation (6). In order to obtain a multiplier/divider with an output equal to (3) we used three of these cells. Each of these cells performs the operation of equation (6) with a different input current. In this sense, we considered three input currents: $I_x + I_y$, $I_x$ and $I_y$. Using these input currents we obtain equations (7), (8), and (9). These equations represent the outputs of the three basic translineal cells used by the multiplier/divider.

$$f = \frac{(I_x + I_y)^2}{4I_w} \qquad (7)$$

$$g = \frac{(I_x)^2}{4I_w} \qquad (8)$$

$$h = \frac{(I_y)^2}{4I_w} \qquad (9)$$

Once that the functions $f$, $g$, and $h$ were defined in terms of the input currents, it is possible to substitute equations (7), (8)

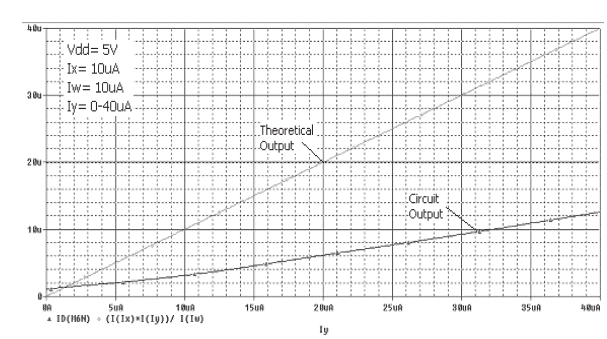


**Fig.6.** Simulation output of the multiplier/divider presented in [6] under the simulation conditions used in [3].

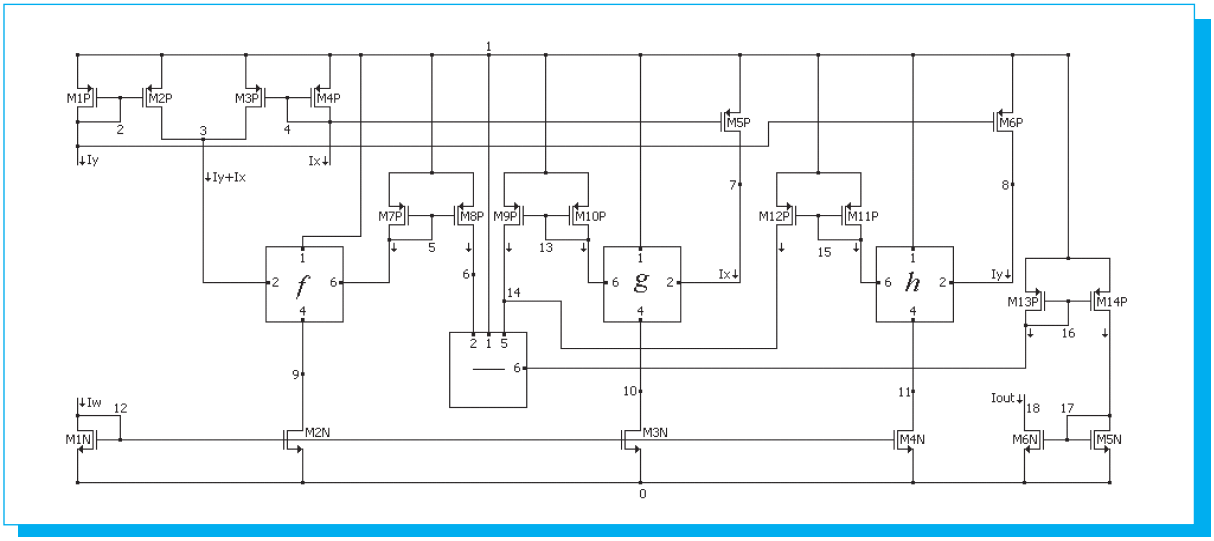


**Fig. 7.** Proposed quadratic-translinear multiplier/divider.

and (9) into equation (10) that becomes the total output of the circuit.

$$I_{out} = 2(f - g - h) = \frac{I_x I_y}{I_w} \qquad (10)$$

As shown in Fig. 6, there is a significant error between the expected output, and the real circuit response. It is important to mention, that the topology proposed in [6] is not the only one able to perform multiplication and division operations. Even though the circuits proposed in [17] and [18] are able to perform this operations, the work presented in [6] was preferred over the one proposed in [17], because it does not work in weak inversion. The work presented in [18] was also discarded, since this circuit relies on a higher complexity to perform the needed operations. In this sense, efforts were focused on the improvement of the work presented in [6], so an efficient performance could be obtained from this circuit.

Some modifications to the structure presented in Fig. 5 were necessary. One current mirror was added to the outputs of the basic translinear cells correspondent to functions *g* and *h*. This change served to make load compensation in node 6, but forced the addition of a subtraction cell due to the current direction change that these mirrors introduced. This problem was carried to the output of the current subtract circuit, two more mirrors were necessary to maintain the direction of the output of the circuit as stated in [6].

In addition, it was necessary to change the geometrical relationships of transistors $M_1N$, $M_2N$, $M_3N$ and $M_4N$ for the basic translinear cells to be able to work properly. In this case, the relationship established for the transistors just mentioned was 3.6 µ/ 0.36 µ. The dimensions of all the other transistors were kept to 0.36 µ/ 0.36 µ, transistor $M_6N$ kept a relationship of 0.72 µ/ 0.36 µ in order to comply with (10).

The image shown in Fig.8 represents the output obtained from the simulation after the modifications previously mentioned were done. Fig. 8 shows a response that follows closely the expected output in a range of 0 to 140 µA. Hence, the modifications proposed in this work improve considerably the performance of the circuit when it is compared with the results obtained in [3].

*C. Circuit for S-Z Shapes.*

The circuit presented next is the basic fuzzy cell for the construction of membership functions [3]; this cell delivers in

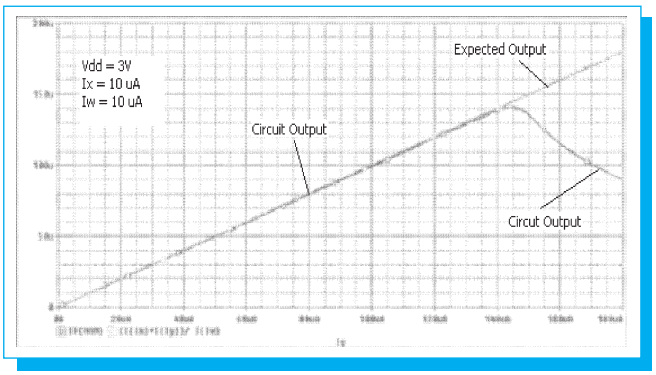


**Fig. 8.** Simulation output after proposed modifications.

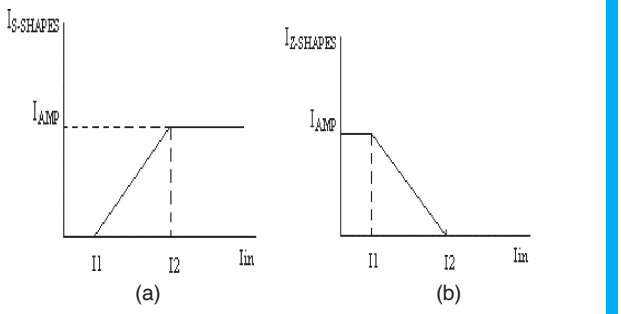


**Fig. 9.** (a) *S* Shape and (b) *Z* shape.

its outputs *S* and *Z* functions depending on the input parameters I1 and I2. For its implementation, we considered the lineal behavior presented by the *S-Z* forms described in [3], this can be seen in Fig. 9.

The models that describe the *S-Z* shapes in Fig. 9 are described next according to [3], and defined as shown by equations (11) and (12). These equations define the structure of the circuit depicted in Fig 10.

$$f(x)_{S-SHAPES} = \begin{bmatrix} I_{Amp} - I_{Amp}\left(1 - \dfrac{I_{in} - I_1}{I_2 - I_1}\right), & I_1 < I_{in} \le I_2 \\ I_{Amp}, & I_{in} > I_2 \\ 0, & I_1 > I_{in} \end{bmatrix} \quad (11)$$

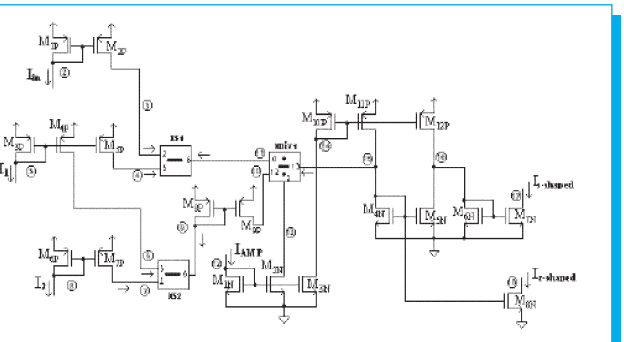

**Fig. 10.** *S-Z* shapes circuit presented in [3].

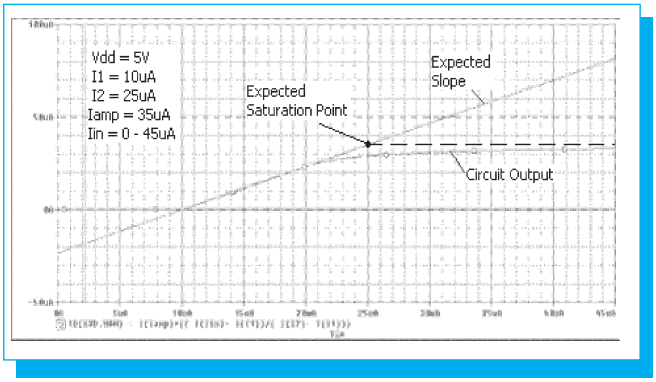


**Fig. 11.** Output error of the *S-Z* shapes circuit.

$$f(x)_{Z-SHAPES} = \begin{bmatrix} I_{Amp}\left(1 - \dfrac{I_{in} - I_1}{I_2 - I_1}\right), & I_1 < I_{in} \le I_2 \\ 0, & I_{in} > I_2 \\ I_{Amp}, & I_1 > I_{in} \end{bmatrix} \quad (12)$$

Functioning errors were found in the structure presented by Fig. 10. The output of the multiplier/divider circuit presented a high error due to a load unbalance in node 15. The same problem was found in node 16. These two nodes were used to make current subtractions in order to comply with (11) and (12). The solution found was to a use current substract subcircuit, instead of doing the substraction in the node. Fig 11 shows the simulation of the *S-Z* shapes circuit presented in [3].

Additional changes were necessary to obtain an efficient circuit performance. Besides the structural modifications, some of the geometrical relationships needed to be changed. Table 2 shows a list of the geometrical relationships necessary for the circuit to operate properly. In this case, all the P-type transistors use the same relationship; the modifications were needed mostly in the N-type transistor's dimensions to adjust the mirror's gain.

The results of the adjustments made to the circuit proposed in [3] can be seen in Fig. 13. Under the new conditions, the circuit delivers *S* and *Z* shapes according to the input parameters, eliminating the error shown in Fig. 11.

*D. TMF Circuit*

There are various methods for the generation of trapezoidal membership functions. Many authors have reported their

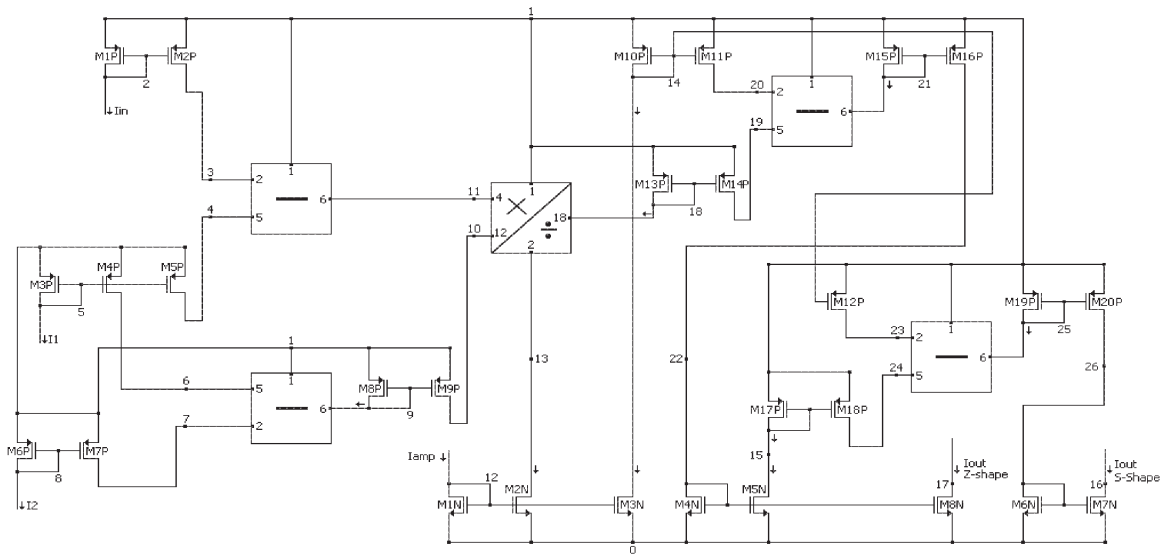


**Fig.12.** Improved *S-Z* shapes circuit.

designs in multiple publications; these include [8,12]. Some of these designs, like [8,10], present very simple structures that have a very reduced implementation area, nevertheless, the poor programmability offered by these designs, puts them in clear disadvantage against the options proposed in [11] and [12].

The work presented in [11] offers the desired programmability, but its implementation is done with BiCMOS technology. The design proposed in [12] is the most similar to the work presented in [3], with the disadvantage that it is unable to deliver trapezoidal and triangular functions with the same circuit.

Besides, the TMF circuit of Camacho is able to generate asymmetric and symmetric membership functions, the structure of the TMF and the parameters that define it are depicted in Fig. 14.

The versatility and high programmability degree offered by the TMF circuit proposed in [3], gives us enough arguments to continue working with this circuit, with the objective to improve its performance. In this case, the TMF is obtained from the subtraction of a *S* shape function from a second *S* shape function.

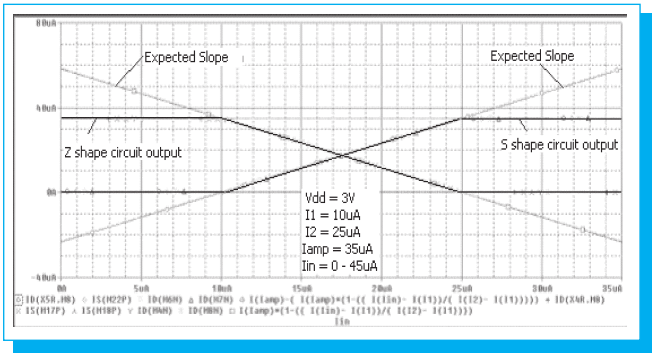


**Fig 13.** Simulation of the proposed *S-Z* shapes circuit.

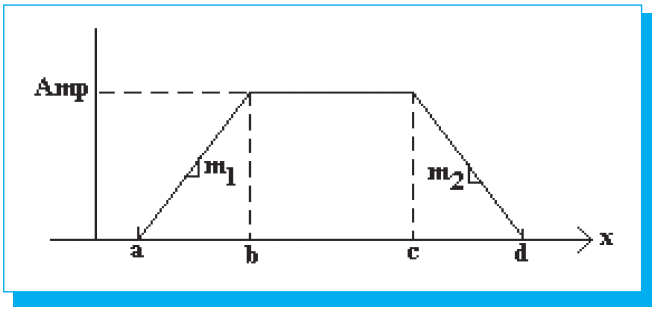


**Fig. 14.** TMF defined by parameters *a, b, c* and *d*.

**Table 2.** Geometrical relationships for the S-Z shapes circuit.

| Transistor | Geometrical Relationship |
|---|---|
| P-type | 0.72µ/0.72µ |
| $M_1N,\ M_2N,\ M_3N$ | 0.36µ/0.36µ |
| $M_4N,\ M_5N,\ M_8N$ | 3.6µ/0.36µ |
| $M_6N,\ M_7N,$ | 0.32µ/0.32µ |

The input parameters described in Fig. 14 define both *S* shaped functions. This is illustrated clearly in Fig. 15.

In this sense, the TMF circuit is formed basically by two *S-Z* shapes subcircuits, in combination with a current substraction. The mathematical model that describes this behavior is defined as

$$I_{TMF} = \left| I_{AMP} - I_{AMP}\left| (1 - \frac{I_{in} - I_a}{I_b - I_a}) \right| \right| - \left| I_{Amp} - I_{Amp}\,(1 - \frac{I_{in} - I_c}{I_d - I_c}) \right| \quad (13)$$

Fig. 16 shows the schematic that represents the TMF circuit. Since the performance of all the cells that compose the TMF

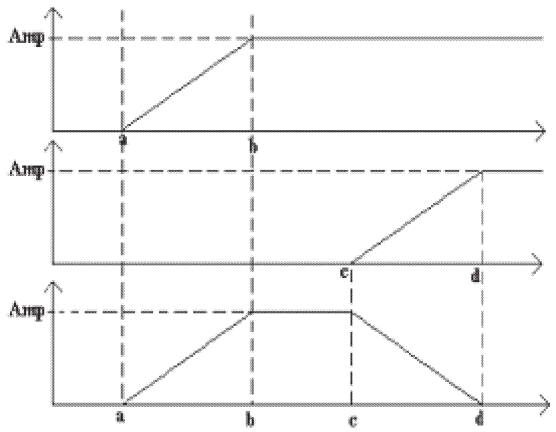


**Fig. 15.** TMF circuit graphical description.

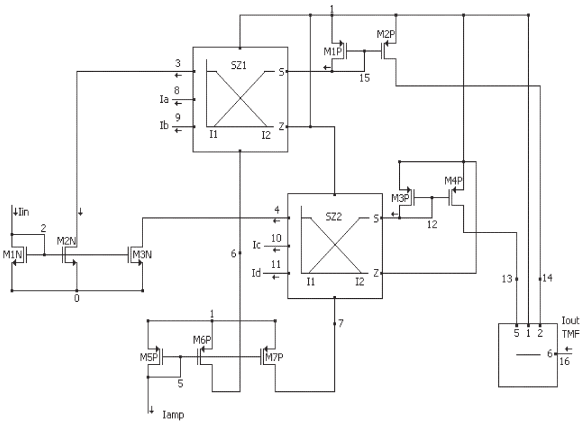


**Fig. 16.** TMF circuit proposed in [3].

circuit were previously improved, we considered that the possible error in the circuit's output should be minimal.

Figure 17 shows the simulation output for the asymmetrical trapezoidal membership function. If the value of current Ia is adjusted, the circuit then delivers a symmetrical trapezoidal function, as it is shown in Fig. 18. In the same manner, if the values of Ib and Ic are equivalent, then the circuit shows a symmetrical triangular function in its output, like the one in Fig. 19. Finally, if the value of Ia is adjusted, the TMF cell then delivers the asymmetrical triangular function depicted in Fig. 20. With this, it is possible to observe that the circuit output can be programmed or controlled via the input parameters $I_a$, $I_b$, $I_c$ and $I_d$. The geometrical relationships used were of 0.36µ/0.36µ for the N-type transistors, and of 0.72µ/0.72µ for the P-

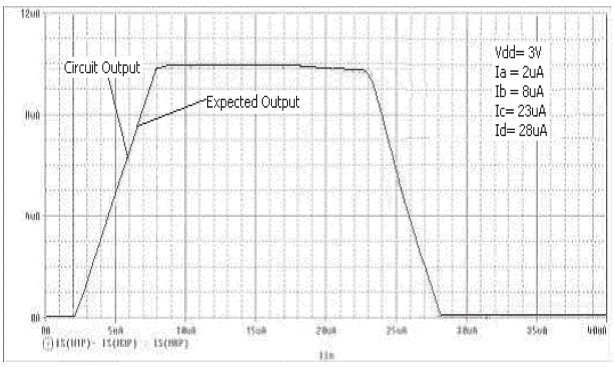


**Fig. 17.**

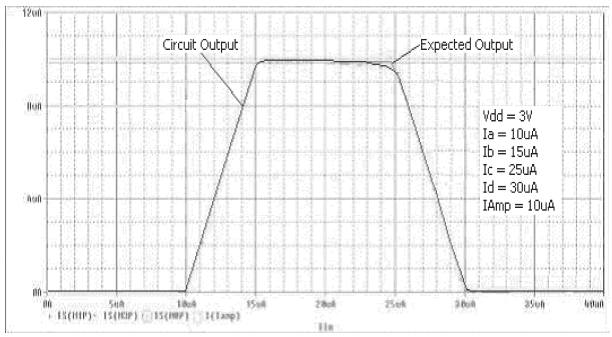


**Fig. 18.** Symmetrical trapezoidal membership function.

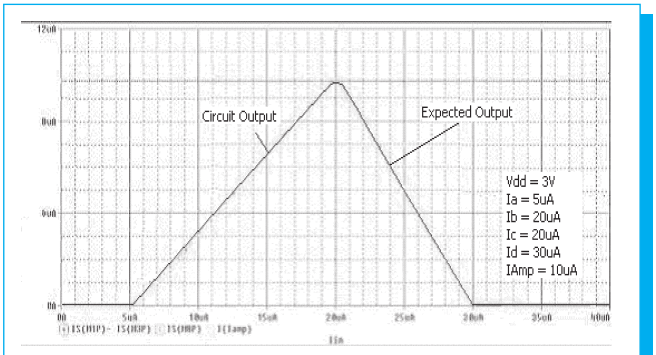


**Fig. 20.** Asymmetrical triangular membership function.

type transistors. The performance of the TMF circuit proposed in this work is much more efficient that the one obtained in [3]. The modifications done to this circuit makes it a proper option in the implementation of a fuzzy system.

## 4.2. Maximum and Minimum Detection Circuits

The maximum and minimum detection circuits are necessary for the implementation of the decision making system based on the Mamdani inference method. In this section we will describe the operation procedure of these circuits.

*A. Maximum Detection Circuit*

Two options were considered for the maximum detection circuit. The first one was proposed in [7], but it was discarded because it only works properly with two inputs. The circuit presented in [5] maintains a stable behavior with many inputs, and is the selected circuit for this work.

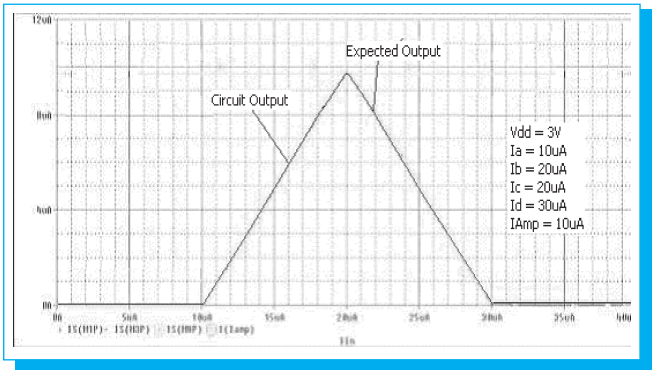


**Fig. 19.** Symmetrical triangular membership function.

The image in Fig. 21 represents the basic cell for the maximum detection circuit. This circuit is based on a very simple operation and the cascade connection of various circuits of this kind composes the maximum detection circuit. The voltage in node 4 is associated directly with the input current In1 and the saturation of $M_2N$ is dependent of this voltage. At the same time, the voltage in node 4 is copied to node 3, therefore the saturation of $M_1N$ and $M_3N$ depends also of this voltage. In summary, the voltage in node 4 controls the saturation of all the transistors in the circuit. The mirror formed by $M_1N$ and $M_3N$ is used to reflect current In1 into node 4.

A maximum detection circuit with two inputs is presented in Fig. 22. As shown in the image, this circuit is composed of two of the basic cells described in Fig.21. In this case, the voltage in node 4 is associated with the maximum input current flowing

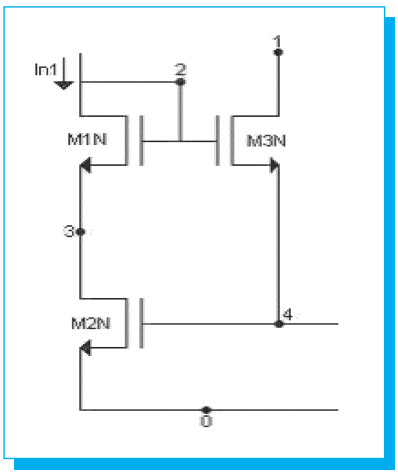


**Fig. 21.** Basic cell for the maximum detection circuit.

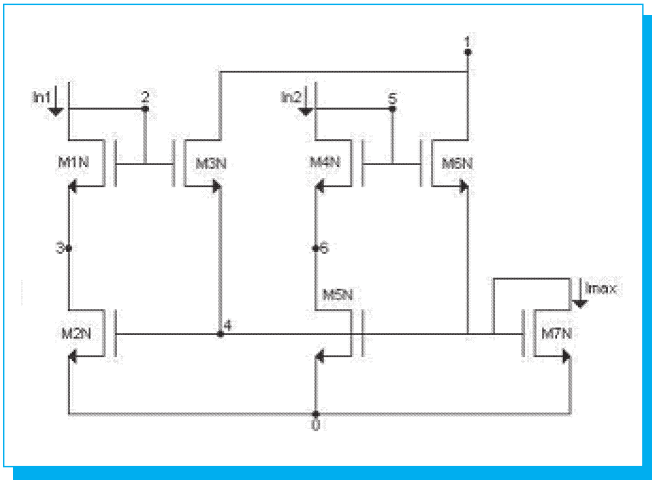


**Fig. 22.** Maximum detection circuit with two inputs.

in the circuit; this makes that only one basic cell works in the saturation region, and the rest in the triode region. Hypothetically speaking, if $I_{n2} > I_{n1}$ then the voltage in node 4 is associated with $I_{n2}$, and as a result, transistors $M_4N$, $M_5N$, and $M_6N$ are in saturation. As a consequence, transistors $M_1N$, $M_2N$ and $M_3N$ are in the triode region, because the voltage in node 4, in this moment, is not related with $I_{n1}$. This is how the circuit is able to discriminate the maximum input current from the rest. Transistor $M_7N$, operating as a diode, is added to replace a current source used in [5]. The circuit output is taken from the drain of $M_7N$. The simulation of the circuit presented in Fig. 22 is shown in Fig.23. This image shows that while $I_{n1} > I_{n2}$ the output is equal to $I_{n1}$, when $I_{n2} > I_{n1}$ the situation is

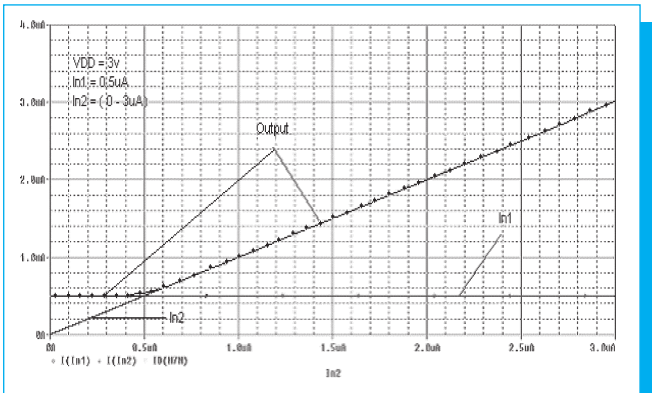


**Fig. 23.** Simulation output of the two input maximum detection circuit.

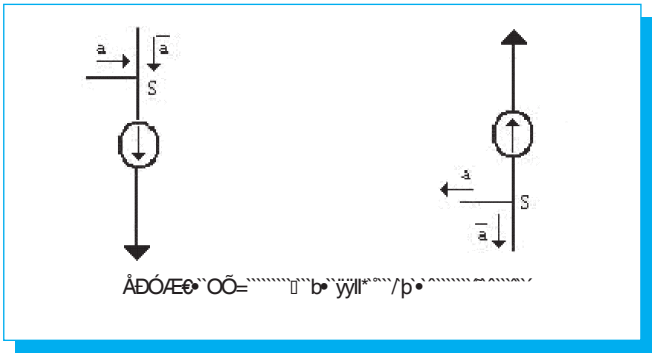


**Fig. 24.** Complement (a) Positive (b) Negative.

reversed, and now the output of the circuit delivers $I_{n2}$ as depicted in the graphic.

The minimum detection circuit is obtained complementing the maximum detection circuit. In terms of fuzzy logic, connective circuits are used for the implementation of the MIN connector between the antecedent rules, according to De Morgan's law using the following expression [21]:

$$\text{Min}(I_1,...,I_n) = \text{Max}(I_1,...,I_n) = I_{ref} - \text{Max}(I_{ref} - I_1,...,I_{ref} - I_n) \quad (14)$$

*B. Minimum Detection Circuit*

Therefore, the minimum current is obtained as the complement of the maximum of the complements. The minimum detection operator can be implemented by complement subcircuits connected to the n inputs and to the output of the maximum

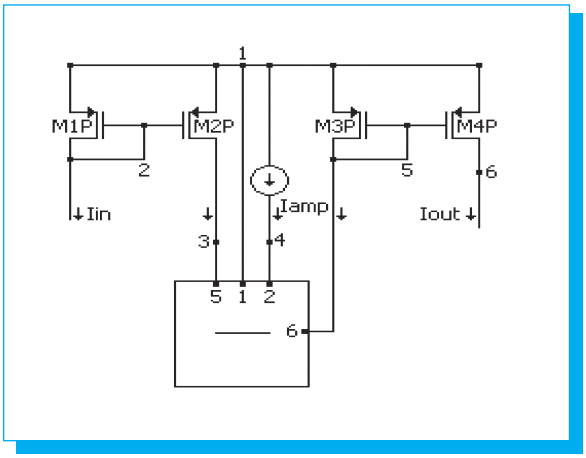


**Fig. 25.** Complement circuit.

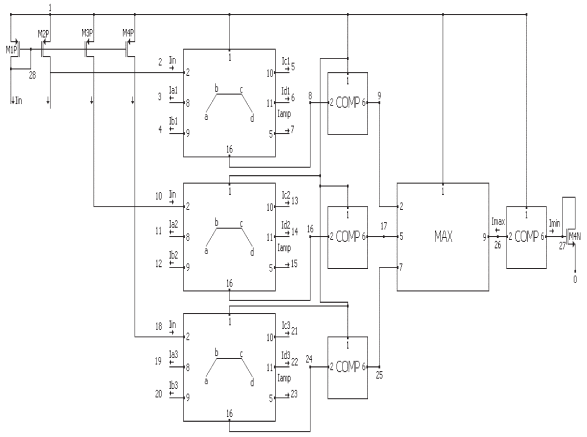


**Fig. 26.** Circuit used for the simulation of the minimum detection circuit.

detection circuit. The complement operation can be easily performed in current-mode applying Kirchoff's current law to node S in Fig. 24. There are two types of complements, positive when the current is entering to S and negative when the current is going out from S. In this case we used a positive complement circuit shown in Fig. 25.

We stated before, that the minimum detection circuit is implemented complementing the inputs and the output of the maximum circuit. This is depicted in the image of Fig. 25. We used three TMF cells as the inputs of the MAX cell in the diagram. As it can be seen, the three inputs and the output of the MAX cell are complemented to form the minimum detection circuit. The parameters that define the

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Iin | 28 | 0 | 1u | Ib2 | 12 | 0 | 13u |
| Iamp1 | 7 | 0 | 10u | Ib3 | 20 | 0 | 16u |
| Iamp2 | 15 | 0 | 10u | Ic1 | 5 | 0 | 15u |
| Iamp3 | 23 | 0 | 10u | Ic2 | 13 | 0 | 18u |
| Ia1 | 3 | 0 | 5u | Ic3 | 21 | 0 | 21u |
| Ia2 | 11 | 0 | 8u | Id1 | 6 | 0 | 20u |
| Ia3 | 19 | 0 | 11u | Id2 | 14 | 0 | 23u |
| Ib1 | 4 | 0 | 10u | Id3 | 22 | 0 | 26u |

**Fig. 27.** Simulation parameters for the input TMFs used in the Fig. 26.

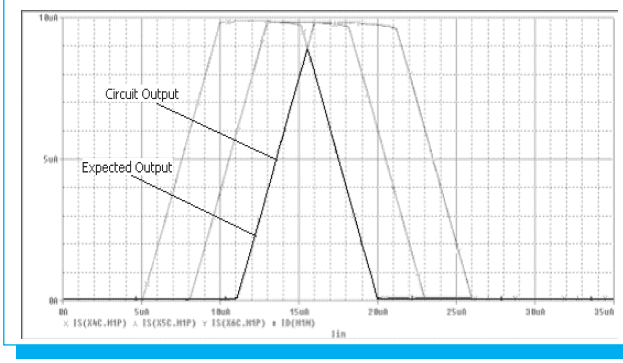


**Fig. 28** Simulation output for the minimum detection circuit

three TMF's are shown in Fig. 27, the feeding voltage used in this simulation was $V_{dd} = 5$ V.

The simulation of Fig. 28 shows that the proposed complement circuit enables the maximum circuit to perform minimum detection operations. As it can be observed in the image, the circuit is able to determine the minimum of the three TMFs that served as inputs. Nevertheless, a problem was found, the maximum detection circuit presents difficulties when all the basic cells in its structure share the same maximum current. In this case, the output is formed by the sum of all the inputs, resulting in a considerable error. This error is eliminated by adjusting the gain of the mirror used in each basic cell for the maximum detection circuit. Since we used a three input maximum circuit, we adjusted the geometrical relationship of transistor $M_3N$ of Fig. 21 to 0.36 μ/1μ for every basic cell used in the circuit. Under these conditions the circuit operates as shown in Fig. 28.

## 4.3 Case of Study: Decision Making System

In this section, the cells described in past sections will be taken for the implementation of a fuzzy decision making system. This structure is based on a Mamdani inference method (MIN-MAZ Inference). The objective of this section is to demonstrate that the proposed cells operate efficiently as part of a fuzzy inference system, in this case, for the water temperature regulation in a bathroom shower.

*A. Mamdani Inference Method*

The Mamdani inference method is used commonly for its simplicity and high implementation efficacy, this method is also known as MIN-MAX inference. It uses the MIN t-norm as the implication function and a MAX s-norm as the aggregation operator [1].

**Table 3.** Input-Output relationship for the decision making system.

If **water temperature** and **ambient temperature** then **cold water tap condition**

| | Water Temperature | AmbientTemperature | Cold Water Tap Condition |
|---|---|---|---|
| 1 | Cold | Cold | Close a lot |
| 2 | Warm | Cold | Close a little |
| 3 | Cold | Warm | Close a little |
| 4 | Warm | Warm | Do nothing |
| 5 | Hot | Cold | Open a little |
| 6 | Cold | Hot | Open a little |
| 7 | Warm | Hot | Open a little |
| 8 | Hot | Hot | Open a lot |
| 9 | Hot | Warm | Open a lot |

This method is an inference mechanism based on base rules of the form

$$\begin{aligned} &\text{Rule 1: if } x_1 \text{ is } A_1^1 \text{ and } x_2 \text{ is } A_2^1 \text{ then } y \text{ is } B^1 \\ &\text{Rule 2: if } x_1 \text{ is } A_1^2 \text{ and } x_2 \text{ is } A_2^2 \text{ then } y \text{ is } B^2 \end{aligned} \quad (15)$$

The inferred conclusion, in the form of a membership function, after the application of the base rules is given by [1]:

$$\mu_B'(y) = \max(\min(\alpha^r, \mu_B^r(y))) \quad (16)$$

Where the activation degree of the r-rule is:

$$\alpha^r = \min(\mu_{A1}^r(x_{01}), \ldots \mu_{An}^r(x_{0n})) \quad (17)$$

*B. Decision Making System: Water Temperature Regulation in a Bathroom Shower.*

The decision making system designed to prove the operation of these cells, pretends to maintain warm the temperature of the water in the shower, regardless of the input state and

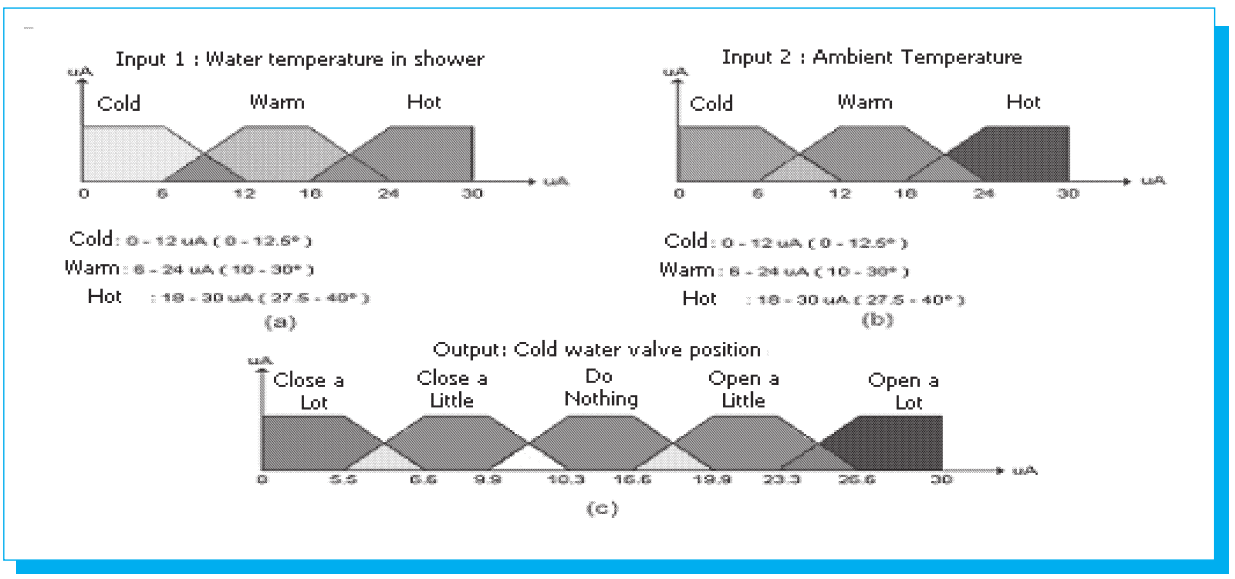


**Fig 29.** Membership functions for (a) Temperature in Shower (b) Ambient Temperature and (c) Output.

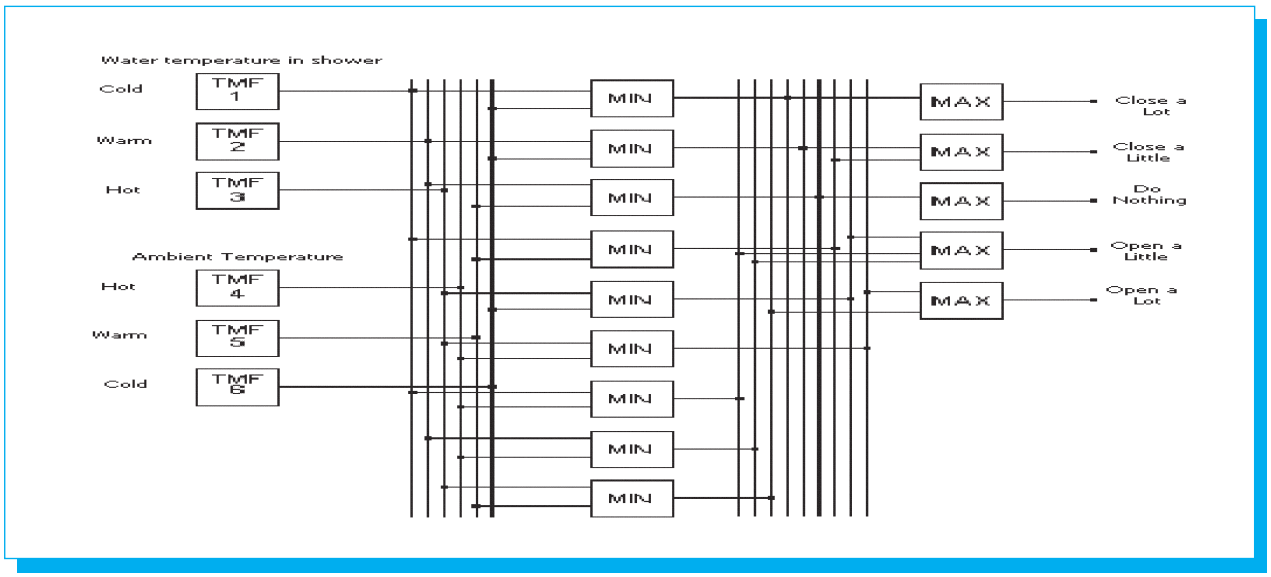


**Fig. 30.** Decision making system block diagram.

supposing that hot water valve is always opened and with constant temperature. In this system, constructed with linguistic sentences, it was established that for the water temperature regulation in a daily bath, a person considers that the input signals are the temperature of the water in the shower and the ambient temperature. Taking in count this input variables, a person takes control actions modifying the position of the cold water tap.

Table 3 shows the series of base rules, and the established relationships between the input signals and the expected output signals. Fig. 29 shows graphically the variable ranges

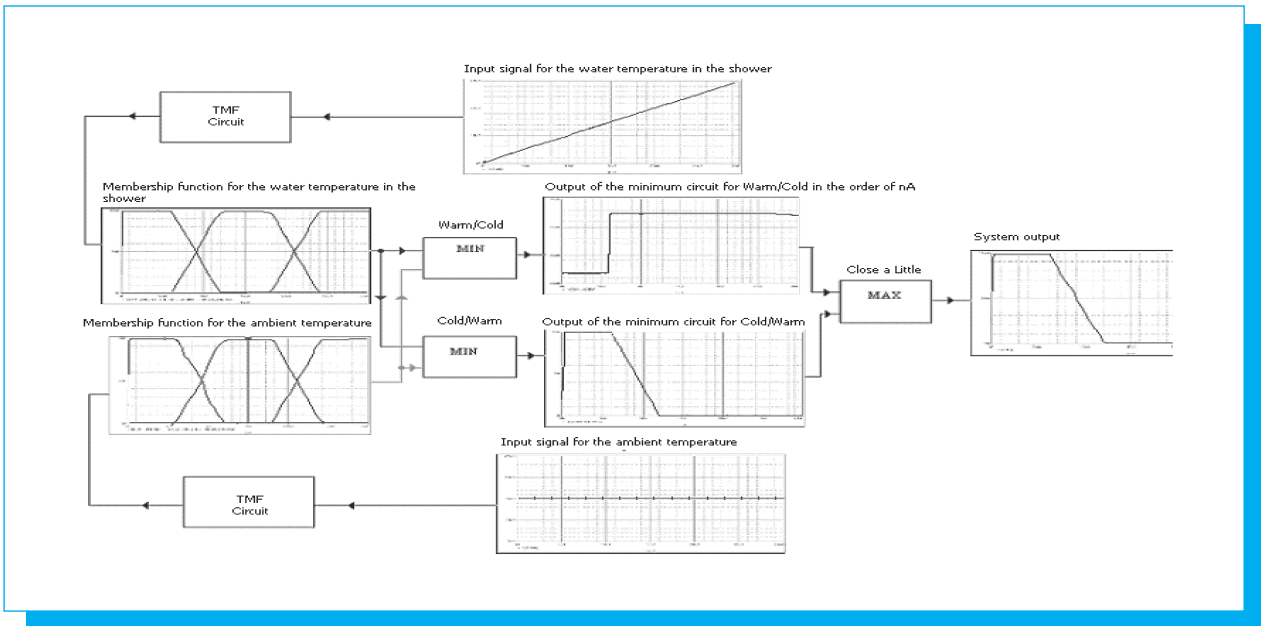


**Fig. 31.** Stage representation of the decision making system.

**Table 4.** Performance of the circuits used in the proposed decision making system, a comparison.

| P-type MOSFET | Feeding voltage | Dynamic range | Power consumption |
|---|---|---|---|
| | 1 V | 0 - 20 µA | 0.0794 mW |
| 2 | 3 V | 0 - 190 µA | 0.240 mW |
| | 5 V | 0 - 400 µA | 0.4 mW |
| | 1 V | 0 - 30 µA | 0.121 mW |
| 20 | 3 V | 0 - 140 µA | 0.364 mW |
| | 5 V | 0 - 240 µA | 0.66 mW |
| | 1 V | 0 - 250 µA | 9 e-5 W |
| 0 | 3 V | 0 - 2.2 µA | 5.43 mW |
| | 5 V | 0 - 6.2 µA | 40.1 mW |
| | 1 V | 0 - 250 µA | 7.22 e-5 mW |
| 0 | 3 V | 0 - 2.2 µA | 17.1 mW |
| | 5 V | 0 - 6.2 µA | 62 mW |
| | 1 V | 0 - 20 µA | 0.31 mW |
| 18 | 3 V | 0 - 130 µA | 6.22 mW |
| | 5 V | 0 - 260 µA | 20.7 mW |
| | 1 V | 0 - 50 µA | 1.17 mW |
| 103 | 3 V | 0 - 50 µA | 3.61 mW |
| | 5 V | 0 - 60 µA | 6.89 mW |

considered. The membership functions that represent the knowledge base are established by means of the relationships stated in Table 3.

In this case, the operating range of the system is defined between 0 and 30 µA. All the membership functions that represent a system input must be defined in this range. Fig. 29a and Fig. 29b show the different membership functions that represent the system inputs. There are three conditions to represent the water temperature in the shower, three for the ambient temperature, and departing from these, the five conditions that represent the system outputs are obtained.

Fig. 30 shows the block diagram for the implementation of the base rules listed in Table 3. The combination for the relationships between the two input variables require nine minimum detection circuits, one for each base rule, and one maximum detection circuit per action to perform. We must add that one input dependent outputs do not require a maximum detection circuit.

Every connection point between the TMF cells and the minimum detection blocks, represent an output reflected by a current mirror in order to direct the output signal to the next block. This condition is not applied between the minimum and maximum detection circuits.

Figure 31 shows the operation of the water regulation system in a graphic way. In this example, the operations done correspond to rules two and three of Table 3. As shown in the image, the operations start with the membership function generation for the system inputs. The input correspondent to the shower is a current sweep that goes from 0 to 30 µA. In this case, only the TMF output representing «cold» is considered, this can be seen in Fig.29a. In the other hand, the input correspondent to the ambient temperature was maintained constant with a value of 15 µA, representing «warm». At the same time, the «warm/cold» input condition is being evaluated. These two conditions «cold/warm» and «warm/cold» give the same answer.

The relationship between antecedents is established via the minimum detection circuit to obtain partial answers that are aggregated in the maximum detection stage. In this way, the output of the minimum detection circuit that corresponds to the input with the highest value will be the output of the entire system. This is shown in Fig. 31, where all the operations are performed with the required efficiency. It is important to add, that the addition of a current mirror at the TMF cells output was necessary to couple this stage with the minimum detection circuits.

To prove the operation decision making system, we tested one by one, the series of base rules defined in Table 3, but for practical reasons we only include the simulation of one example in this work. For every case, the system delivered the expected output for a given input combination. With this efficient circuit operation, we conclude that the modifications made to the circuits described in past sections, make the proposed cells suitable for their utilization in more complex systems.

## 5. Conclusions

This work presents a significant improvement in the performance of the cells initially proposed by Camacho in [3]. In first instance, the technology used was scaled from 0.8µm AMS to 0.18µm. This change represents a great improvement in terms of circuit area utilization; it allows the utilization of the proposed cells in systems that require a minimal circuit layout area. In the same way, the errors that caused an inefficient circuit operation, were identified and corrected. All topologies presented an improved performance after the proposed modifications, in some cases the error was reduced to noise levels. It becomes obvious, that the inefficient operation of one cell is translated into a functioning error in the consequent cell, affecting the entire system performance. This exposes the existent dependency between the system cells.

Table 4 presents a performance comparison of the circuits used in this work under different feeding conditions. In most cases the dynamic range of the proposed cells doubles the one obtained in [3]. At the same time, the power consumption

was reduced to half of the one registered by Camacho's work. In the other hand, the maximum and minimum circuits present simple topologies with a stable operation with multiple inputs. These circuits are very important, since the operation of the inference system is based on their efficient performance.

The fuzzy cell proposed in this work present an efficient operation in individual manner, and as part of a complex system. The TMF circuit offers a clear advantage over the other designs, since it is able to generate programmable symmetrical and asymmetrical membership functions. It also shows a greater flexibility by being constituted by independent cells, same that can be replaced with more efficient topologies, as it was done in this work.

The decision making system not only proved the efficient performance of the proposed cells, it also demonstrated the precision with which a fuzzy system is able to obtain conclusions using rules, that are based on linguistic variables that manage uncertain information.

The improvement of the cells proposed in [3], and the use of the maximum and minimum detection circuits allowed the implementation of a fuzzy inference system. It is important to mention, that the decision making system designed in this work is not the only possibility, these group of circuits permit the creation of a n-rule system with any decision purpose.

Since, this work corresponds only to the fuzzification stage, it is objective of a further work, the creation of a fuzzy VLSI processor that controls the input parameters of the membership functions, which represent the knowledge base, and that is also able to manipulate, with the use of analog switches, the rule configuration and the associative fuzzy matrix. Another action line for the future is the study of the proposed topologies with an analysis perspective of geometrical change sensitivities, mismatches, noise, total harmonic distortion, source noise rejection, in other words, the parametric optimization of the designs. The collection of circuits presented in this work, allows the realization of an integrated circuit with specific application in an area of less than 3mm2, including the needed fuzzy processor and the defuzzification stage .

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